## Code No.: 15432 S

## VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD

Accredited by NAAC with A++ Grade

## B.E. (E.C.E.) V-Semester Supplementary Examinations, June-2022 Integrated Circuits and Applications

Time: 3 hours

Max. Marks: 60

Note: Answer all questions from Part-A and any FIVE from Part-B

Part-A  $(10 \times 2 = 20 \text{ Marks})$ 

Q. No.	Stem of the question	M	L	CO	PO
1.	What is the value of Vo in the circuit given in the figure below?  V <sub>1</sub> =2V  O V <sub>0</sub>	2	3	1	1,2
	V <sub>2</sub> =3V +				
2.	Give the expression for total output offset voltage of an Operational amplifier?	2	2	1	1
3.	State the merits and demerits of active filters over passive filters.	2	1	2	1
4.	What is the role of control voltage in timer IC 555?	2	2	2	1
5.	How many bits are required to design a D/A converter that can have a resolution of 5mv? The ladder has +8V full scale.	2	3	3	1,2
6.	Draw the pin-out diagram of a variable voltage regulator and state what the amount of reference.	2	2	3	1
7.	Mention the drawbacks of standard TTL logic family.	2	1	4	1
8.	List out the characteristics of CMOS logic.	2	1	4	1
9.	Draw 4bit magnitude comparator.	2	2	5	1
10.	Explain how shift register can be converted into ring counter and Johnson counter with the logic diagram.	2	2	5	1
	Part- $B$ (5×8 = 40 Marks)				
11. a)	Briefly explain the necessity and function of different stages of OP-AMP with respect toits block schematic?	4	2	1	1
b)	For an OP-AMP having a Slew rate of $3V/\mu s$ . What is the maximum closed loop voltage gain that can be used when the input signal varies by $0.4 \text{ v}$ in $12 \mu s$ ?	4	4	1	1,
12. a)	Design first order high pass filter at a cut-off frequency of 400Hz and a pass band gain of 2, by specifying the assumptions taken into considerations?	4	3	2	1
b)	Design and explain the Function Generators using IC 8038.	4	2	2	

		-		
Draw the internal diagram of IC-723 voltage regulator and explain its functionality.	4	1	3	1
Explain the operation of a 3-bit R-2Rtype DAC and the expression for the output voltage.	4	2	3	1
Draw and explain NAND gate operation using CMOS logic.	4	3	4	1
Explain how to interface TTL with CMOS logic.	4	. 1	4	1
Design a Parallel Binary Adder/Subtractor using 2's Complement method.	5	3	5	2
Design a binary up counter using IC 74XX series.	3	3	5	2
Show that the output of the subtractor is proportional to the difference between the two input voltages?	3	2	1	1
Derive the transfer function, gain, and phase angle for first order and second order low pass active filter.	5	2	2	1
Answer any two of the following:				
The basic step of a 9-bit DAC is 10.3mV. If 00000000 represents 0V	4	3	3	1,2
i) Find the output of a DAC for an input: 101101101 and 011011011				
What is the full scale reading of this DAC?				
Draw and explain the operation of tristate TTL inverter.	4	1	4	1
Design mod 5 Asynchronous counter.	4	3	5	2
	functionality.  Explain the operation of a 3-bit R-2Rtype DAC and the expression for the output voltage.  Draw and explain NAND gate operation using CMOS logic.  Explain how to interface TTL with CMOS logic.  Design a Parallel Binary Adder/Subtractor using 2's Complement method.  Design a binary up counter using IC 74XX series.  Show that the output of the subtractor is proportional to the difference between the two input voltages?  Derive the transfer function, gain, and phase angle for first order and second order low pass active filter.  Answer any two of the following:  The basic step of a 9-bit DAC is 10.3mV. If 000000000 represents 0V  i) Find the output of a DAC for an input: 101101101 and 011011011  What is the full scale reading of this DAC?  Draw and explain the operation of tristate TTL inverter.	functionality.  Explain the operation of a 3-bit R-2Rtype DAC and the expression for the output voltage.  Draw and explain NAND gate operation using CMOS logic.  Explain how to interface TTL with CMOS logic.  Design a Parallel Binary Adder/Subtractor using 2's Complement method.  Design a binary up counter using IC 74XX series.  3 Show that the output of the subtractor is proportional to the difference between the two input voltages?  Derive the transfer function, gain, and phase angle for first order and second order low pass active filter.  Answer any two of the following:  The basic step of a 9-bit DAC is 10.3mV. If 000000000 represents 0V  i) Find the output of a DAC for an input: 101101101 and 011011011  What is the full scale reading of this DAC?  Draw and explain the operation of tristate TTL inverter.	functionality.  Explain the operation of a 3-bit R-2Rtype DAC and the expression for the output voltage.  Draw and explain NAND gate operation using CMOS logic.  Explain how to interface TTL with CMOS logic.  Design a Parallel Binary Adder/Subtractor using 2's Complement method.  Design a binary up counter using IC 74XX series.  Show that the output of the subtractor is proportional to the difference between the two input voltages?  Derive the transfer function, gain, and phase angle for first order and second order low pass active filter.  Answer any two of the following:  The basic step of a 9-bit DAC is 10.3mV. If 000000000 represents 0V  i) Find the output of a DAC for an input: 101101101 and 011011011  What is the full scale reading of this DAC?  Draw and explain the operation of tristate TTL inverter.  4 1	functionality.  Explain the operation of a 3-bit R-2Rtype DAC and the expression for the output voltage.  Draw and explain NAND gate operation using CMOS logic.  Explain how to interface TTL with CMOS logic.  Design a Parallel Binary Adder/Subtractor using 2's Complement method.  Design a binary up counter using IC 74XX series.  Show that the output of the subtractor is proportional to the difference between the two input voltages?  Derive the transfer function, gain, and phase angle for first order and second order low pass active filter.  Answer any two of the following:  The basic step of a 9-bit DAC is 10.3mV. If 000000000 represents 0V  i) Find the output of a DAC for an input: 101101101 and 011011011  What is the full scale reading of this DAC?  Draw and explain the operation of tristate TTL inverter.  4 1 4

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	22.50%
i)	Blooms Taxonomy Level – 2	37.50%
iii)	Blooms Taxonomy Level – 3 & 4	40%

\*\*\*\*